phase of the second clock such as to fix a relative phase difference between the phase adjustment signal and the first clock, wherein

each of said semiconductor devices is a semiconductor memory device including an output buffer from which data stored in memory cells is output in synchronism with the second clock.

A copy of the marked up amended claims is attached to this response showing the changes as set forth in 37 C.F.R. § 1.121.

REMARKS

Claims 2 and 4-27 are pending in this application. By this Amendment, claims 1 and 3 have been cancelled and the subject matter incorporated into claims 2 and 4 respectively. Claims 5 and 15-23 have merely been amended to depend from claim 4. Claim 25 has been amended to more particularly point out and distinctly claim the invention. No new matter is added. Claims 29-33 remain withdrawn from further consideration.

This reply is submitted as a complete response to the outstanding Office Action. Reconsideration of the application in view of the above amendments and following remarks is respectfully requested.

The Office Action asserted that the non-elected claims must be cancelled. However, Applicant is unaware of any requirement to cancel non-elected claims before the time of allowance. Therefore, Applicants respectfully request clarification of the Examiner's position.

The Office Action rejected claims 1-6, 15-18, 20 and 22-24 under 35 U.S.C. § 102(e) as being anticipated by Ries et al. (U.S. Patent No. 5,734,877, "Ries"). (Although

the Office Action asserted that the AIPA of 1999 does not apply to the present application, Applicant respectfully submits that the changes should apply because the present application was filed June 6, 2001). By this amendment, claims 1 and 3 have been cancelled and the subject matter incorporated into claims 2 and 4, respectively. Therefore, the rejection as to these claims is moot. However, applicant respectfully submits that claims 2, 4-6, 5-18, 20 and 22-24 recite subject matter that is neither disclosed nor suggested in Ries.

Claim 2 recites a module including a semiconductor device. A phase adjustment circuit receives a phase adjustment signal output from the semiconductor device and a first clock supplied from an exterior of the module, and generates a second clock. An output circuit provided in the semiconductor device generates the phase adjustment signal from the second clock. The phase adjustment circuit adjusts a phase of the second clock so as to fix a relative phase difference between the phase adjustment signal and the first clock. The semiconductor device is a semiconductor memory device including an output buffer from which data stored in memory cells is output in synchronism with the second clock.

Claim 4 recites a module including semiconductor devices. One of the devices is a first semiconductor device that outputs a phase adjustment signal. A phase adjustment circuit receives the phase adjustment signal output from the first semiconductor device and a first clock supplied from an exterior of the module, and generates a second clock, the second clock being supplied to the semiconductor devices. A wiring board is provided on which the semiconductor devices and the phase adjustment circuit are mounted. The first semiconductor device includes an output circuit which generates the phase adjustment signal from the second clock. The phase adjustment circuit adjusts a phase of the second

clock such as to fix a relative phase difference between the phase adjustment signal and the first clock. Each of the semiconductor devices is a semiconductor memory device including an output buffer from which data in memory cells is output in synchronism with the second clock.

In making this rejection, the Office Action took the position that Ries discloses all of the elements of the claimed invention. However, it is respectfully submitted that the prior art fails to disclose or suggest the structure of the claimed invention, and therefore, fails to provide the advantages of the present invention. For example, the module of the present invention is a semiconductor memory device including an output buffer from which data stored in memory cells are output in synchronism with the second clock.

With this claimed arrangement, the output data and the second clock can be accurately synchronized with each other without being affected by noise superimposed on a power supply thereto.

Ries discloses a processor chip 15. A master clock generator 17 sends a clock signal to the processor chip 15 which has a clock generation circuitry 30 which generates a number of clock signals for use by the processor circuitry. The clock generation circuitry 30 includes an internal clock generator 32 and an external clock generator 35. The internal clock generator 32 includes a phase-lock loop (PLL) 40, a clock divider 42, and an initial synchronization circuit 45. A plurality of remote synchronization circuits 50 are located at a plurality of distributed regions on the chip. The generated plurality of clock signals (referred to as 1x, 2x and 4x and a pair of additional signals PLL1x and Sync4x) are synchronized and distributed to the remote regions, where they are again synchronized to

Sync4x. The synchronized PLL1x signal from one of the remote locations is fed back as a signal SyncPLL to a second input of the PLL 40 for overall synchronization.

The Office Action took the position that the remote synchronization circuit 50 of Ries is equivalent to the semiconductor device of the present invention. However, the Applicant respectfully disagrees because it appears that the remote synchronization circuit 50 is provided solely for the purpose of supplying clock signals after establishing synchronization of the clock signals at each remote location. That is, the remote synchronization circuit 50 is simply a mechanism for establishing clock synchronization at each remote location, and is never intended to output its own data signals. On the contrary, the semiconductor device of the present invention is a semiconductor memory device that includes an output buffer from which data in memory cells are output in synchronism with the second clock, as recited in claims 2 and 4.

Furthermore, assuming *arguendo*, if the remote synchronization circuit 50 of Ries is a semiconductor memory device that outputs data signals stored in its memory cells, the system as taught by Ries could not operate since the function to establish clock synchronization at each remote location would be lost.

Thus, in view of the above, Applicant respectfully submits that Ries does not disclose or suggest all the claimed features of Applicant's invention.

Therefore, it is respectfully submitted that the Applicant's invention, as set forth in claims 2 and 4 is not anticipated within the meaning of 35 U.S.C. § 102.

As claims 5, 15-18 and 21-24 depend from claim 4, Applicant respectfully submits that each of these claims incorporate the patentable aspects thereof, and are therefore allowable for at least the same reasons as discussed above.

Claims 7-14, 19, 21 and 25-27 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Ries. However, Applicant respectfully submits that claims 7-14, 19, 21 and 25-27 recite subject matter that is neither disclosed nor suggested in Ries.

Claim 25 recites a system including modules, a wiring board on which the modules are mounted, and a dummy output load line serving as loads of dummy output data output from the modules. The modules comprise a module including, semiconductor devices, one of which is a first semiconductor device that outputs a phase adjustment signal, a phase adjustment circuit which receives the phase adjustment signal output from the first semiconductor device and a first clock supplied from an exterior of the module, and generates a second clock, the second clock being supplied to the semiconductor devices, and a wiring board on which the semiconductor devices and the phase adjustment circuit are mounted. The first semiconductor device includes an output circuit for generating the phase adjustment signal from the second clock. The phase adjustment circuit adjusts a phase of the second clock such as to fix a relative phase difference from the phase adjustment signal and the first clock. Each of the semiconductor devices is a semiconductor memory device including an output buffer from which data stored in memory cells are output in synchronism with the second clock.

In making this rejection, the Office Action took the position that Ries discloses all the elements of the claimed invention, except for disclosing how the first and second data lines are arranged. However, as discussed above, Applicant submits that Ries fails to disclose or suggest a semiconductor memory device including an output buffer from which data in memory cells are output in synchronism with the second clock.

Therefore, it is respectfully submitted that the Applicant's invention, as forth in claims 7-14, 19, 21 and 25-27 is not obvious within the meaning of 35 U.S.C. § 103.

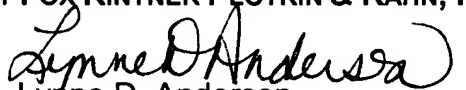
Still further, because claims 7-1, 19 and 21 depend directly or indirectly on claim 4, and claims 26 and 27 depend on claim 25, Applicant submits that that these claims recite subject matter that is neither disclosed nor suggested by the cited prior art, for at least the reasons set forth above with respect to the independent claims.

In view of the above remarks, Applicant respectfully submits that this application is in condition for allowance. Favorable consideration and prompt allowance of claims is earnestly solicited. If the application is still not in condition for allowance, the Examiner is invited to contact Applicant's undersigned attorney at the telephone number listed below.

In the event this paper is not considered to be timely filed, Applicant respectfully petitions for an appropriate extension of time. The Commissioner is authorized to charge payment for any additional fees which may be required with respect to this paper to Counsel's Deposit Account 01-2300, referring to docket number 100353-00064.

Respectfully submitted,

ARENT FOX KINTNER PLOTKIN & KAHN, PLLC



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Enclosures: Marked-Up Copy of Amended Claims

MARKED-UP COPY OF AMENDED CLAIMS

2. (Amended) [The module as claimed in claim 1,] A module comprising:

a semiconductor device;

a phase adjustment circuit which receives a phase adjustment signal output from said semiconductor device and a first clock supplied from an exterior of said module, and generates a second clock; and

an output circuit that is provided in the semiconductor device and generates the phase adjustment signal from the second clock, wherein said phase adjustment circuit adjusts a phase of the second clock such as to fix relative phase difference between the phase adjustment signal and the first clock, wherein

said semiconductor device is a semiconductor memory device including an output buffer from which data stored in memory cells are output in synchronism with the second clock.

4. (Amended) [The module as claimed in claim 3,] A module comprising:

semiconductor devices;

a phase adjustment circuit generating a second clock so that a phase adjustment signal output from a first semiconductor device that is one of the semiconductor devices and a first clock have a predetermined phase relationship, the second clock being supplied to the semiconductor devices; and

a wiring board on which the semiconductor devices and the phase adjustment circuit are mounted,

the first semiconductor device including an output circuit generating the phase adjustment signal from the second clock, wherein said phase adjustment circuit adjusts a

phase of the second clock such as to fix a relative phase difference between the phase adjustment signal and the first clock, wherein

each of said semiconductor devices is a semiconductor memory device including an output buffer from which data in memory cells are output in synchronism with the second clock.

5. (Amended) The module as claimed in claim [3] 4, wherein the module comprises first data lines over which data output from the semiconductor devices are transferred, and a second data line over which the phase adjustment signal output from the first semiconductor device is transferred,

the first and second data lines being provided on the wiring board.

15. (Amended) The module as claimed in claim [3] 4, further comprising a terminal that is provided on the wiring board and is used to output the phase adjustment signal to an outside of the module.

16. (Amended) The module as claimed in claim [3] 4, wherein the first semiconductor device generates the phase adjustment signal in accordance with a predetermined signal given from an outside of the first semiconductor device.

17. (Amended) The module as claimed in claim [3] 4, wherein:

the semiconductor devices including the first semiconductor device have an identical circuit configuration; and

the first semiconductor device has an output circuit that receives an external instruction that instructs the first semiconductor device to generate the phase adjustment signal.

18. (Amended) The module as claimed in claim [3] 4, wherein the first clock is

supplied from an outside of the module.

19. (Amended) The module as claimed in claim [3] 4, further comprising a circuit generating the first clock from an external clock.

20. (Amended) The module as claimed in claim [3] 4, wherein each of the semiconductor devices comprises a programmable delay circuit that delays the second clock.

21. (Amended) The module as claimed in claim [3] 4, wherein the semiconductor devices comprise semiconductor memory devices.

22. (Amended) The module as claimed in claim [3] 4, wherein the phase adjustment circuit generates the second clock from dummy output data output by the first semiconductor device.

23. (Amended) The module as claimed in claim [3] 4, further comprising a second phase adjustment circuit generating a third clock so that the third clock and the first clock have a predetermined phase relationship, the third clock being supplied to the semiconductor devices.

25. (Twice Amended) A system comprising:

modules;

a wiring board on which the modules are mounted; and

a dummy output load line serving as loads of dummy output data output from the modules, wherein the modules comprise a module including;

a semiconductor devices, one of which is a first semiconductor device that outputs a phase adjustment signal;

a phase adjustment circuit which receives the phase adjustment signal output from said first semiconductor device and a first clock supplied from an exterior of said module, and generates a second clock, the second clock being supplied to the semiconductor devices; and

a wiring board on which the semiconductor devices and the phase adjustment circuit are mounted,

the first semiconductor device including an output circuit generating the phase adjustment signal from the second clock, wherein said phase adjustment circuit adjusts a phase of the second clock such as to fix a relative phase difference between the phase adjustment signal and the first clock, wherein

each of said semiconductor devices is a semiconductor memory device including an output buffer from which data stored in memory cells are output in synchronism with the second clock.